COMP: Computer Architecture for Game Devices

Module Title:	Computer Architecture for Game Devices
Language of Instruction:	English

Credits:	5

NFQ Level:	6

Module Delivered In	1 programme(s)

Teaching & Learning Strategies:	Combination of lecture and laboratory sessions. Lectures will provide traditional theory. Laboratory sessions will employ formative practical/assessment sheets.

Module Aim:	Explore the structure, role and function of components that constitute a computer system. Examine the architecture of a computer system including constituent components, buses, memory and CPU.

Learning Outcomes	
On successful completion of this module the learner should be able to:	
LO1	Identify the architectural components of a computer, and understand the role of each component and inter-connector
LO2	Understand and differentiate between hardware, software and firmware

Pre-requisite learning
Module Recommendations *This is prior learning (or a practical skill) that is recommended before enrolment in this module.*
No recommendations listed
Incompatible Modules *These are modules which have learning outcomes that are too similar to the learning outcomes of this module.*
No incompatible modules listed
Co-requisite Modules
No Co-requisite modules listed
Requirements *This is prior learning (or a practical skill) that is mandatory before enrolment in this module is allowed.*
No requirements listed

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Module Content & Assessment

Indicative Content
Number Systems and Data Representation Understanding and using numbers expressed in different bases. Unsigned and signed data types, addition and subtraction, floating-point representation, precision and accuracy and character storage ASCII and Floating Points
Logic Logic, Logic Gates and Circuits Flip flops, Adders and Decoders Analogue/Digital; Switching elements; Logic gates; Logic circuits, types and examples.
Software Models Introduction to the layers of software / firmware architecture
Memory RAM / ROM, Primary memory: organisation and operation; cache. Computer memory: Types, costs, organization and operation, speed. Data storage devices

Assessment Breakdown	%
Project	30.00%
Practical	20.00%
End of Module Formal Examination	50.00%

No Continuous Assessment

Project

Assessment Type	*Assessment Description*	*Outcome addressed*	*% of total*	*Assessment Date*
Project	Logic Circuit		30.00	Week 22

Practical

Assessment Type	*Assessment Description*	*Outcome addressed*	*% of total*	*Assessment Date*
Practical/Skills Evaluation	Laboratory based practicals	1,2	20.00	Every Week

End of Module Formal Examination

Assessment Type	*Assessment Description*	*Outcome addressed*	*% of total*	*Assessment Date*
Formal Exam	No Description	1,2	50.00	End-of-Semester

SETU Carlow Campus reserves the right to alter the nature and timings of assessment

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Module Workload

Workload: Full Time		
Workload Type	*Frequency*	*Average Weekly Learner Workload*
Lecture	12 Weeks per Stage	1.00
Laboratory	12 Weeks per Stage	2.00
Estimated Learner Hours	15 Weeks per Stage	5.93
	Total Hours	125.00

Module Delivered In

Programme Code	Programme	Semester	Delivery
CW_KCCGD_B	Bachelor of Science (Honours) in Computer Games Development	3	Mandatory