DIGT: Digital Logic

Module Title:	Digital Logic
Language of Instruction:	English

Credits:	5

NFQ Level:	6

Module Delivered In	3 programme(s)

Teaching & Learning Strategies:	Students will be assessed by means of Continuous Assessment.

Module Aim:	To provide the student with an appreciation for digital logic.

Learning Outcomes	
On successful completion of this module the learner should be able to:	
LO1	Understand computer representation such as integer, floating point and character.
LO2	Understand fundamental concepts of digital logic design including basic and universal gates.
LO3	Analyze small-scale combinational and sequential circuits.

Pre-requisite learning
Module Recommendations *This is prior learning (or a practical skill) that is recommended before enrolment in this module.*
No recommendations listed
Incompatible Modules *These are modules which have learning outcomes that are too similar to the learning outcomes of this module.*
No incompatible modules listed
Co-requisite Modules
No Co-requisite modules listed
Requirements *This is prior learning (or a practical skill) that is mandatory before enrolment in this module is allowed.*
No requirements listed

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Module Content & Assessment

Indicative Content
Data representation Data representation: Twos complement format; IEEE floating point format, ASCII, EBCDIC and Unicode.
Introduction to digital logic. Basic gates. Simple sequential circuits.
Boolean axioms and theorems Identity Property, Idempotent Property, Complement Property De morgans theorem
Adders Half-adder, full adder, 4 bit ripple adder.
Karnaugh Maps Simplification of logic using K-maps
Decoders 2-4 decoder, 3-8 decoder
Multiplexers 1x2 Multiplexer, 1x4 Multiplexer
Latches and Flip Flops S-R Latch, D flip flop, J-K flip flop
7 segment display Illustrate the logic behind a 7 segment display
Counters 2 bit counter, 3 bit counter
Memory 1 bit memory, 4 x 4 memory
SAP-1 computer Overview of SAP-1 computer

Assessment Breakdown	%
Continuous Assessment	100.00%

Continuous Assessment				
Assessment Type	*Assessment Description*	*Outcome addressed*	*% of total*	*Assessment Date*
Other	In class and/or in lab continuous assessment	1,2,3	100.00	n/a

No Project

No Practical

No End of Module Formal Examination

SETU Carlow Campus reserves the right to alter the nature and timings of assessment

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Module Workload

Workload: Full Time		
Workload Type	*Frequency*	*Average Weekly Learner Workload*
Lecture	12 Weeks per Stage	3.00
Laboratory	12 Weeks per Stage	2.00
Estimated Learner Hours	15 Weeks per Stage	4.33
	Total Hours	125.00

Module Delivered In

Programme Code	Programme	Semester	Delivery
CW_KCSOF_B	Bachelor of Science (Honours) in Software Development	3	Mandatory
CW_KCSOF_D	Bachelor of Science in Software Development	3	Mandatory
CW_KCCOM_C	Higher Certificate in Science in Computing Programming	3	Mandatory