SETU
Ollscoil Teicneolaíochta an Oirdheiscirt
South East Technological University

ZCOM H2201: Computer Architecture

Module Title:	Computer Architecture

Credits:	10

NFQ Level:	6

Module Delivered In	No Programmes

Teaching & Learning Strategies:	Students will be assessed by means of Continuous Assessment and Final Examination. The Continuous Assessment component will consist of practical tests and theory tests.

Module Aim:	To enable the student to program in assembly and to provide the student with a good knowledge of computer architecture.

Learning Outcomes	
On successful completion of this module the learner should be able to:	
LO1	Program in 80X86 assembly language;
LO2	Pass parameters using the stack;
LO3	Select the appropriate addressing mode to accomplish a given task;
LO4	Interpret logic circuits;
LO5	Describe the workings of computer architecture as addressed in the syllabus;

Pre-requisite learning
Module Recommendations *This is prior learning (or a practical skill) that is recommended before enrolment in this module.*
No recommendations listed
Incompatible Modules *These are modules which have learning outcomes that are too similar to the learning outcomes of this module.*
No incompatible modules listed
Co-requisite Modules
No Co-requisite modules listed
Requirements *This is prior learning (or a practical skill) that is mandatory before enrolment in this module is allowed.*
No requirements listed

Module Content & Assessment

Indicative Content
Assembly Language Programming Programming: Generic machine language view; Introduction to microprocessors; 80X86 machine and assembly language programming; Addressing modes. Data representation: Integers, character storage, ASCII, EBCDIC and Unicode; Character I/O; Arrays; Strings. Comparison of assembler and high-level language: Examine assembler versions of simple HLL programs. Stack usage; Subroutines internal & external; Parameter passing.
Computer Architecture Logic circuits: Gates, adder, latches, memory circuit. Addressing methods review: Register, immediate, direct, register indirect, base plus index, register relative, base relative plus index. Addressing support for high level languages: Activation records; local and non-local data . Computer structure: CPU architecture, fetch execute cycle, buses. Interrupts and interrupt handlers; Vectored interrupts, internal/external h/w interrupts, s/w interrupts, interrupt vector table, ISR. I/O systems: Programmed, Interrupt driven and DMA; DMA controller . CISC and RISC architectures; Acceleration and Concurrency: Pipelining, instruction prefetching, instruction queues, cache memory. Introduction to parallel architectures: Array processors; Multiprocessors; Multicomputers; SISD, SIMD, MISD, MIMD. Fundamentals of current processors. Mobile computing: Typical pipeline on mobile processor;Out-of-order architectures;ARM Big.Little Architecture. Structured assembly programming: lab work augmenting the theoretical aspects.

Assessment Breakdown	%
Continuous Assessment	50.00%
End of Module Formal Examination	50.00%

Continuous Assessment				
Assessment Type	*Assessment Description*	*Outcome addressed*	*% of total*	*Assessment Date*
Other	In Class and/or In Lab Continuous Assessment	1,2,3,4,5	50.00	n/a

No Project

No Practical

End of Module Formal Examination				
Assessment Type	*Assessment Description*	*Outcome addressed*	*% of total*	*Assessment Date*
Formal Exam	Formal Final Exam	1,2,3,4,5	50.00	End-of-Semester

SETU Carlow Campus reserves the right to alter the nature and timings of assessment

Module Workload

Workload: Full Time

Workload Type	*Frequency*	*Average Weekly Learner Workload*
Lecture	30 Weeks per Stage	3.00
Laboratory	30 Weeks per Stage	2.00
Estimated Learner Hours	30 Weeks per Stage	1.67
	Total Hours	200.00