

Module Title:	Hardware Description Language
Language of Instruction:	English
Credits:	5
NFQ Level:	8
Module Delivered In	2 programme(s)
Teaching & Learning Strategies:	A combination of lectures, class discussion, tutorial, laboratory exercises and demonstrations will be used. Emphasis will be placed on active learning including problem / project bases learning.
Module Aim:	To provide learners with the knowledge and skills needed to design, simulate, synthesis and validate a digital circuit using a contemporary hardware description language (HDL).
Learning Outcomes	
<i>On successful completion of this module the learner should be able to:</i>	
LO1	Use a Hardware Description Language (HDL) to synthesize combinational and sequential logic.
LO2	Use a Hardware Description Language (HDL) to create a test bench to simulate and validate a small digital system which incorporates combinational and sequential logic
LO3	Design and implement a finite state machine (FSM) using a hardware description language (HDL).
LO4	Interface an FPGA to seven segment displays, Leds and mechanical switches (which are to be debounced).
Pre-requisite learning	
Module Recommendations <i>This is prior learning (or a practical skill) that is recommended before enrolment in this module.</i>	
No recommendations listed	
Incompatible Modules <i>These are modules which have learning outcomes that are too similar to the learning outcomes of this module.</i>	
No incompatible modules listed	
Co-requisite Modules	
No Co-requisite modules listed	
Requirements <i>This is prior learning (or a practical skill) that is mandatory before enrolment in this module is allowed.</i>	
No requirements listed	

Module Content & Assessment

Indicative Content

Logic synthesis:

Logic synthesis using a MUX or LUT. Structure and operation of an FPGA.

Modelling techniques:

Gate-level, dataflow & behavioural modelling of digital systems. Combinational circuits – mux, decoder, priority encoder etc. Sequential circuits – registers, RAM, shift registers, counters etc Structural description of a hierarchical system. Synchronous design techniques.

HDL Language:

Lexical elements: comments, identifiers, numbers, strings etc. Data types: nets, registers, vectors, arrays. Operators, branching, looping etc. Procedural assignments: blocking and non-blocking. Sequential logic and event-based behaviour.

Finite state machine:

ASM charts, Moor & mealy machines, FSM encoding (one hot etc), HDL description of an FSM.

Design reuse:

Economic benefits of design reuse. Parameterized models. IP. Libraries. Supporting documentation and testbench.

Introduction to design verification:

Ethical and economic motivation for design verification. Develop a basic test bench for combinational circuits (adder) or sequential circuits (pre-settable up/down counter). Generating and assigning test vectors. Instance of design under test (DUT). Reporting test results. Tasks and functions.

Systems issues:

Implications of design techniques for power, speed, timing and area. Static timing analysis. Debouncing transient signals from switches etc

Assessment Breakdown	%
Continuous Assessment	50.00%
Project	25.00%
Practical	25.00%

Continuous Assessment

Assessment Type	Assessment Description	Outcome addressed	% of total	Assessment Date
Case Studies	n/a	1,2,3	50.00	n/a

Project

Assessment Type	Assessment Description	Outcome addressed	% of total	Assessment Date
Project	n/a	1,2,3,4	25.00	n/a

Practical

Assessment Type	Assessment Description	Outcome addressed	% of total	Assessment Date
Practical/Skills Evaluation	n/a	1,2,3,4	25.00	n/a

No End of Module Formal Examination

SETU Carlow Campus reserves the right to alter the nature and timings of assessment

Module Workload

Workload: Full Time		
<i>Workload Type</i>	<i>Frequency</i>	<i>Average Weekly Learner Workload</i>
Lecture	Every Week	3.00
Practicals	Every Week	2.00
Independent Learning	Every Week	3.00
Total Hours		8.00

Module Delivered In

Programme Code	Programme	Semester	Delivery
CW_EEBEE_B	<u>Bachelor of Engineering (Honours) in Biomedical Electronics</u>	7	Mandatory
CW_EESYS_B	<u>Bachelor of Engineering (Honours) in Electronic Engineering</u>	7	Mandatory