DSGN H4601: Microelectronic Design 2

Module Title:	Microelectronic Design 2
Language of Instruction:	English

Credits:	5

NFQ Level:	8

Module Delivered In	1 programme(s)

Teaching & Learning Strategies:	Teaching will take the form of problem-based learning during tutorials and practical classes. An emphasis will be placed on relating individual circuits and devices to useful practical applications both in theory and practical classes. Circuit simulation software will be used extensively in the problem-solving sessions to validate students' solutions.

Module Aim:	To provide: (a) Detailed analyses of semiconductor devices and their CAD models. (b) Knowledge of circuit-level simulation and layout tools. (c) Methodologies for digital and analogue IC analysis and design.

Learning Outcomes	
On successful completion of this module the learner should be able to:	
LO1	Design and analyse the frequency response of analogue integrated circuits.
LO2	Design and analyse analogue ICs utilising negative feedback.
LO3	Design and analyse combinational and sequential digital CMOS circuits.
LO4	Design and analyse mixed-signal ICs.

Pre-requisite learning
Module Recommendations *This is prior learning (or a practical skill) that is recommended before enrolment in this module.*
No recommendations listed
Incompatible Modules *These are modules which have learning outcomes that are too similar to the learning outcomes of this module.*
No incompatible modules listed
Co-requisite Modules
No Co-requisite modules listed
Requirements *This is prior learning (or a practical skill) that is mandatory before enrolment in this module is allowed.*
Students should have completed a module equivalent to the following from CW558: Microelectronic Design 1 (yr4).

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Module Content & Assessment

Indicative Content
1. Frequency Response High-Frequency Device Modelling; Frequency Response of CE and CS Stages; Frequency Response of CC and CD Stages; Frequency Response of Cascode and Differential Stages.
2. Feedback Properties of Negative Feedback; Feedback Topologies; Effect of Non-ideal I/O Impedances; Stability in Feedback Systems.
3. Digital CMOS Cells Static and Dynamic Characterisation of Gates; CMOS Inverter; Static CMOS Logic Design; Power and Delay Considerations; Static Sequential Cell Design.
4. Mixed-Signal Circuits ADC and DAC Circuits; Switched-Capacitor Comparator; PLLs.

Assessment Breakdown	%
Continuous Assessment	20.00%
Practical	20.00%
End of Module Formal Examination	60.00%

Continuous Assessment

Assessment Type	*Assessment Description*	*Outcome addressed*	*% of total*	*Assessment Date*
Examination	Students will sit a written examination during the module.	1,2,3	20.00	n/a

No Project

Practical

Assessment Type	*Assessment Description*	*Outcome addressed*	*% of total*	*Assessment Date*
Practical/Skills Evaluation	Students will complete a series of practical assignments, under supervision, using circuit simulation software.	1,2,3,4	20.00	n/a

End of Module Formal Examination

Assessment Type	*Assessment Description*	*Outcome addressed*	*% of total*	*Assessment Date*
Formal Exam	A written examination, at the end of the module, will examine the extent of the student's achievement of the learning outcomes.	1,2,3,4	60.00	End-of-Semester

SETU Carlow Campus reserves the right to alter the nature and timings of assessment

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Module Workload

Workload: Full Time		
Workload Type	*Frequency*	*Average Weekly Learner Workload*
Lecture	Every Week	3.00
Practicals	Every Week	2.00
Independent Learning Time	Every Week	2.00
	Total Hours	7.00

Module Delivered In

Programme Code	Programme	Semester	Delivery
CW_EESYS_B	Bachelor of Engineering (Honours) in Electronic Engineering	8	Mandatory