PROG H3603: Programmable Electronics

Module Title:	Programmable Electronics
Language of Instruction:	English

Credits:	10

NFQ Level:	7

Module Delivered In	No Programmes

Teaching & Learning Strategies:	A combination of lectures, class discussion, tutorials, practicals and demonstrations will be used.

Module Aim:	To give the student the knowledge, competencies and skills to design and implement electronic systems using programmable electronic devices such as microcontrollers and programmable logic devices (PLD).

Learning Outcomes	
On successful completion of this module the learner should be able to:	
LO1	Describe the operation of a microcontroller based embedded computer system and its component parts.
LO2	Interface a microcontroller to peripheral components to form an embedded system.
LO3	Develop and test a programme for a microcontroller based system using contemporary microcontroller development tools.
LO4	Describe the structure of a field programmable gate array (FPGA).
LO5	Develop HDL models of basic combinational and sequential logic which can be implemented using an FPGA and simulated using contemporary FPGA development tools.

Pre-requisite learning
Module Recommendations *This is prior learning (or a practical skill) that is recommended before enrolment in this module.*
No recommendations listed
Incompatible Modules *These are modules which have learning outcomes that are too similar to the learning outcomes of this module.*
No incompatible modules listed
Co-requisite Modules
No Co-requisite modules listed
Requirements *This is prior learning (or a practical skill) that is mandatory before enrolment in this module is allowed.*
No requirements listed

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Module Content & Assessment

Indicative Content
Microcontroller Architecture Architecture of a microcontroller (CPU, ALU, memory and I/O).
Interfacing I/O and interfacing to sensors, switches, displays, shift registers, etc.
Software Development Program development for a microcontroller.
Communications Serial communications, e.g. RS232, SPI, etc.
Interrupts Polling and interrupts, interrupt service routines (ISRs).
Timers Timers and timer interrupts.
Debug Testing and debugging microcontroller based systems, need for test, breakpoints, single stepping, etc.
Logic synthesis Logic synthesis using a MUX or LUT. Structure and operation of a contemporary programmable logic device (PLD) such as an FPGA.
Hardware Description Languages Development of HDL models of basic combinational and sequential logic which can be implemented using an FPGA and simulated using contemporary FPGA development tools.

Assessment Breakdown	%
Continuous Assessment	20.00%
Practical	20.00%
End of Module Formal Examination	60.00%

Continuous Assessment

Assessment Type	*Assessment Description*	*Outcome addressed*	*% of total*	*Assessment Date*
Examination	Students will be assigned a number of assignments and/or class tests as part of the assessment of this module. Students may be asked to complete assignments during class or as homework.	1,2,3,4,5	20.00	n/a

No Project

Practical

Assessment Type	*Assessment Description*	*Outcome addressed*	*% of total*	*Assessment Date*
Practical/Skills Evaluation	Students will complete practical assignments involving the design, programming and testing of microcontroller based embedded systems. Students will be required to keep a record of practical work and write a brief report on each assignment.	2,3	12.00	Every Week
Practical/Skills Evaluation	Students will complete practical assignments involving the design, programming and testing of FPGA based digital circuits. Students will be required to keep a record of practical work and write a brief report on each assignment.	5	8.00	Every Week

End of Module Formal Examination

Assessment Type	*Assessment Description*	*Outcome addressed*	*% of total*	*Assessment Date*
Formal Exam	A final written examination will assess learning outcomes.	1,2,3,4,5	60.00	End-of-Semester

SETU Carlow Campus reserves the right to alter the nature and timings of assessment

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Module Workload

Workload: Full Time		
Workload Type	*Frequency*	*Average Weekly Learner Workload*
Lecture	Every Week	3.00
Practicals	Every Week	2.00
Independent Learning	Every Week	3.00
	Total Hours	8.00