GAME H1202: Computer Architecture for Game Devices

Module Title:	Computer Architecture for Games Devices
Credits:	10
NFQ Level:	6
Module Delivered In	No Programmes
Teaching & Learning Strategies:	Combination of lecture and laboratory sessions. Lectures will provide traditional theory. Laboratory sessions will employ formative practical/assessment sheets and learning assembly language. Project work will be based on programming in assembly language on an embedded games device
Module Aim:	Introduce the structure, role and function of components that constitute a computer system. Examine the architecture of a computer system including constituent components, buses, memory, CPU, instruction set of a microprocessor and connected peripherals. Introduce assembly language programming on an embedded games device

Learning Outcomes	
On successful completion of this module the learner should be able to:	
LO1	Identify the architectural components of a computer, and understand the role of each component and inter-connector
LO2	Understand and differentiate between hardware, software and firmware
LO3	Understand the operation of a microprocessor and develop assembly language programs for embedded games devices

Pre-requisite learning
Module Recommendations *This is prior learning (or a practical skill) that is recommended before enrolment in this module.*
No recommendations listed
Incompatible Modules *These are modules which have learning outcomes that are too similar to the learning outcomes of this module.*
No incompatible modules listed
Co-requisite Modules
No Co-requisite modules listed
Requirements *This is prior learning (or a practical skill) that is mandatory before enrolment in this module is allowed.*
No requirements listed

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Module Content & Assessment

Indicative Content
Hardware Introduction to Computer Hardware. Structure of a computer: CPU architecture and operation, memory, I/O; ALU, registers, fetch/execute cycle, and buses. I/O devices.
Number Systems and Data Representation Understanding and using numbers expressed in different bases. Unsigned and signed data types, addition and subtraction, floating-point representation, precision and accuracy and character storage ASCII and Floating Points
Logic Logic, Logic Gates and Circuits Flip flops, Adders and Decoders Analogue/Digital; Switching elements; Logic gates; Logic circuits, types and examples.
Software Models Introduction to the layers of software / firmware architecture
Memory RAM / ROM, Primary memory: organisation and operation; cache. Computer memory: Types, costs, organization and operation, speed. Data storage devices
Assembly Language Introduction to 68000 and 8-bit Atmel Micro-controller ATmega644 processors and instruction sets. Machine language, displaying and modifying of register and memory contents. Instruction sets: characteristics and function, modes and formats, data types, addressing, flow of control.

Assessment Breakdown	%
Continuous Assessment	10.00%
Project	20.00%
Practical	10.00%
End of Module Formal Examination	60.00%

Continuous Assessment

Assessment Type	*Assessment Description*	*Outcome addressed*	*% of total*	*Assessment Date*
Other	Quiz and case study	1,2	10.00	Every Week

Project

Assessment Type	*Assessment Description*	*Outcome addressed*	*% of total*	*Assessment Date*
Project	Assembly Programming	3	20.00	Week 22

Practical

Assessment Type	*Assessment Description*	*Outcome addressed*	*% of total*	*Assessment Date*
Practical/Skills Evaluation	Laboratory based practicals	1,2	10.00	Every Second Week

End of Module Formal Examination

Assessment Type	*Assessment Description*	*Outcome addressed*	*% of total*	*Assessment Date*
Formal Exam	No Description	1,2,3	60.00	End-of-Semester

SETU Carlow Campus reserves the right to alter the nature and timings of assessment

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Module Workload

Workload: Full Time		
Workload Type	*Frequency*	*Average Weekly Learner Workload*
Lecture	30 Weeks per Stage	1.50
Laboratory	30 Weeks per Stage	1.00
Estimated Learner Hours	30 Weeks per Stage	2.00
	Total Hours	135.00