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|---------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------|
| <b>Module Title:</b>                                                                                                | Digital Logic                                                                                |
| <b>Language of Instruction:</b>                                                                                     | English                                                                                      |
| <b>Credits:</b>                                                                                                     | 5                                                                                            |
| <b>NFQ Level:</b>                                                                                                   | 6                                                                                            |
| <b>Module Delivered In</b>                                                                                          | <a href="#">3 programme(s)</a>                                                               |
| <b>Teaching &amp; Learning Strategies:</b>                                                                          | Students will be assessed by means of Continuous Assessment.                                 |
| <b>Module Aim:</b>                                                                                                  | To provide the student with an appreciation for digital logic.                               |
| <b>Learning Outcomes</b>                                                                                            |                                                                                              |
| <i>On successful completion of this module the learner should be able to:</i>                                       |                                                                                              |
| LO1                                                                                                                 | Understand computer representation such as integer, floating point and character.            |
| LO2                                                                                                                 | Understand fundamental concepts of digital logic design including basic and universal gates. |
| LO3                                                                                                                 | Analyze small-scale combinational and sequential circuits.                                   |
| <b>Pre-requisite learning</b>                                                                                       |                                                                                              |
| <b>Module Recommendations</b>                                                                                       |                                                                                              |
| <i>This is prior learning (or a practical skill) that is recommended before enrolment in this module.</i>           |                                                                                              |
| No recommendations listed                                                                                           |                                                                                              |
| <b>Incompatible Modules</b>                                                                                         |                                                                                              |
| <i>These are modules which have learning outcomes that are too similar to the learning outcomes of this module.</i> |                                                                                              |
| No incompatible modules listed                                                                                      |                                                                                              |
| <b>Co-requisite Modules</b>                                                                                         |                                                                                              |
| No Co-requisite modules listed                                                                                      |                                                                                              |
| <b>Requirements</b>                                                                                                 |                                                                                              |
| <i>This is prior learning (or a practical skill) that is mandatory before enrolment in this module is allowed.</i>  |                                                                                              |
| No requirements listed                                                                                              |                                                                                              |

**Module Content & Assessment**

| Indicative Content                                                                                                                |
|-----------------------------------------------------------------------------------------------------------------------------------|
| <b>Data representation</b><br>Data representation: Twos complement format; IEEE floating point format, ASCII, EBCDIC and Unicode. |
| <b>Introduction to digital logic.</b><br>Basic gates. Simple sequential circuits.                                                 |
| <b>Boolean axioms and theorems</b><br>Identity Property, Idempotent Property, Complement Property De Morgans theorem              |
| <b>Adders</b><br>Half-adder, full adder, 4 bit ripple adder.                                                                      |
| <b>Karnaugh Maps</b><br>Simplification of logic using K-maps                                                                      |
| <b>Decoders</b><br>2-4 decoder, 3-8 decoder                                                                                       |
| <b>Multiplexers</b><br>1x2 Multiplexer, 1x4 Multiplexer                                                                           |
| <b>Latches and Flip Flops</b><br>S-R Latch, D flip flop, J-K flip flop                                                            |
| <b>7 segment display</b><br>Illustrate the logic behind a 7 segment display                                                       |
| <b>Counters</b><br>2 bit counter, 3 bit counter                                                                                   |
| <b>Memory</b><br>1 bit memory, 4 x 4 memory                                                                                       |
| <b>SAP-1 computer</b><br>Overview of SAP-1 computer                                                                               |

| Assessment Breakdown  | %       |
|-----------------------|---------|
| Continuous Assessment | 100.00% |

| Continuous Assessment |                                              |                   |            |                 |
|-----------------------|----------------------------------------------|-------------------|------------|-----------------|
| Assessment Type       | Assessment Description                       | Outcome addressed | % of total | Assessment Date |
| Other                 | In class and/or in lab continuous assessment | 1,2,3             | 100.00     | n/a             |

No Project

No Practical

No End of Module Formal Examination

SETU Carlow Campus reserves the right to alter the nature and timings of assessment

**Module Workload**

| <b>Workload: Full Time</b> |                    |                                        |
|----------------------------|--------------------|----------------------------------------|
| <i>Workload Type</i>       | <i>Frequency</i>   | <i>Average Weekly Learner Workload</i> |
| Lecture                    | 12 Weeks per Stage | 3.00                                   |
| Laboratory                 | 12 Weeks per Stage | 2.00                                   |
| Estimated Learner Hours    | 15 Weeks per Stage | 4.33                                   |
| Total Hours                |                    | 125.00                                 |

**Module Delivered In**

| Programme Code | Programme                                                              | Semester | Delivery  |
|----------------|------------------------------------------------------------------------|----------|-----------|
| CW_KCSOF_B     | <a href="#">Bachelor of Science (Honours) in Software Development</a>  | 3        | Mandatory |
| CW_KCSOF_D     | <a href="#">Bachelor of Science in Software Development</a>            | 3        | Mandatory |
| CW_KCCOM_C     | <a href="#">Higher Certificate in Science in Computing Programming</a> | 3        | Mandatory |